IN THE SPECIFICATION:

Please amend the second full paragraph appearing on page 2 as follows:

Field of the Invention: The present invention relates to processes for selectively etching doped silicon dioxide that overlies silicon nitride or undoped silicon dioxide. Particularly, the process of the present invention includes an etchant mixture which includes the use of an ethane gas having the general formula $C_2H_xF_y$, where x is an integer from two to five, inclusive, y is an integer from one to four, inclusive, and x plus y ~~equals 6.~~ equals six. The present invention also relates to etchant mixtures which include a component having the general formula $C_2H_xF_y$, where x is an integer from two to five, inclusive, y is an integer from one to four, inclusive, and x plus y ~~equals 6.~~ equals six.

Please amend the second full paragraph appearing on page 3 as follows:

An exemplary wet etch process is disclosed in United States Patent 5,300,463 ("the '463 patent"), issued to David A. Cathey et al. The wet etch process of the '463 patent, which employs hydrofluoric acid (HF) as an etchant, is selective for doped silicon dioxide over undoped silicon dioxide. Despite its specificity, that technique is somewhat undesirable from the standpoint that it suffers from many of the shortcomings that are typically associated with wet etch processes. Specifically, the technique of the '463 patent is an isotropic etch. Consequently, the structures defined thereby have different dimensions than those of the target area of the etch substrate that is exposed through the protective mask. Moreover, as those of skill in the art are aware, since wet etch techniques are typically isotropic, if the thickness of the film being etched is approximately equivalent to the minimum desired pattern dimension, the undercutting that is typically caused by isotropic etching becomes intolerable. Similarly, with the ~~ever-decreasing~~ ever-decreasing size of structures that are carried on the active surfaces of semiconductor devices, etching must be very accurate and maintained within very precise tolerances in order to preserve the alignment of such minute structures and to optimize the electrical characteristics of such structures. Such precision cannot be obtained while defining structures on semiconductor devices with many conventional wet etch processes. Thus, the lack

of precision and isotropic nature of typical wet etching processes are inconsistent with the overall goal of etch processes in forming structures on state-of-the-art semiconductor devices: reproducing the features defined by the protective mask with a high degree of fidelity.

Please amend the paragraph bridging pages 3 and 4 as follows:

In contrast, many dry etch techniques including, without limitation, ~~glow-discharge~~ glow-discharge sputtering, ion milling, reactive ion etching (RIE), reactive ion beam etching (RIBE) and high-density plasma etching, are capable of etching in a substantially anisotropic fashion, meaning that the target area of an etch substrate is etched primarily in a substantially vertical direction relative to the exposed, or active, surface of the etched substrate. Thus, such dry etch techniques are capable of defining structures with substantially upright sidewalls from the etch substrate. Consequently, such dry etch techniques are capable of accurately reproducing the features of a protective mask. Thus, due to ever-decreasing dimensions of structures on semiconductor devices, dry etching is often desirable for defining structures upon semiconductor device active surfaces.

Please amend the third full paragraph appearing on page 4 as follows:

Since the gate structures of many semiconductor devices include a silicon nitride (Si_3N_4) cap, selectivity between silicon dioxide (SiO_2) and silicon nitride is desirable in order to etch contacts through passivation layers. Many of the so-called silicon ~~dioxide-selective~~ dioxide-selective plasma dry etch techniques, however, have a SiO_2 to Si_3N_4 selectivity ratio, or etch rate of SiO_2 to etch rate of Si_3N_4, of less than about 3:1.

Please amend the fourth full paragraph appearing on page 6 as follows:

The etchants of the present invention include $C_2H_xF_y$, where x is an integer from two to five, inclusive, y is an integer from one to four, inclusive, and x plus y ~~equals 6.~~ equals six. Specifically, the $C_2H_xF_y$ component of the present invention may be selected from the group consisting of $C_2H_2F_4$, $C_2H_3F_3$, $C_2H_4F_2$, and C_2H_5F. The $C_2H_xF_y$ component may be used as

either a primary etchant or as a component of an etchant mixture. When employed as a primary etchant, $C_2H_xF_y$ etches doped silicon dioxide at a slow rate relative to the etch rates of many conventional silicon dioxide dry etch techniques, but selectively etches doped silicon dioxide over undoped silicon dioxide.

Please amend the first full paragraph appearing on page 8 as follows:

The doped silicon dioxide etchant of the present invention, which is also merely referred to as an etchant for simplicity, includes an ethane component of the general formula $C_2H_xF_y$, which is also referred to as the $C_2H_xF_y$ component or $C_2H_xF_y$ for simplicity, where x is an integer from two to five, inclusive, y is an integer from one to four, inclusive, and x plus y ~~equals 6.~~ equals six. Specifically, the $C_2H_xF_y$ component of the present invention is desirably selected from the group consisting of $C_2H_2F_4$, $C_2H_3F_3$, $C_2H_4F_2$, and C_2H_5F. The doped silicon dioxide etchant may also include combinations of various types of $C_2H_xF_y$.

Please amend the second full paragraph appearing on page 8 as follows:

As the $C_2H_xF_y$ component of a doped silicon dioxide etchant is RF activated, the hydrogen ions and activated hydrogen species react with the fluorine-containing ions and activated fluorine-containing species (e.g., F* and CF*), removing the activated ~~fluorine-containing~~ fluorine-containing species from the surface of the wafer prior to the occurrence of any substantial amount of etching of an etch stop layer of either undoped silicon dioxide or silicon nitride. The hydrogen content of the $C_2H_xF_y$ additives imparts etchants including the same with specificity for doped silicon dioxide over undoped silicon dioxide.

Please amend the second full paragraph appearing on page 9 as follows:

In another embodiment of the doped silicon dioxide etchant of the present invention, $C_2H_xF_y$ is employed as an additive to one or more primary etchants. $C_2H_xF_y$ may be used as an additive to etchants which include a fluorocarbon primary etchant, such as CF_4, CHF_3, or other fluorocarbons which etch silicon dioxide at a higher rate than they etch silicon nitride (i.e., are

selective for silicon dioxide over silicon nitride). According to ~~the'344~~ the '344 patent, CF_4 and CHF_3 are exemplary primary etchants with which $C_2H_xF_y$ may be utilized as an additive.

Please amend the paragraph bridging pages 10 and 11 as follows:

Referring to FIGs. 1 to 4, the etch process of the present invention, which utilizes the inventive etchant, is illustrated. FIG. 1 depicts an exemplary multi-layer structure 10, which is also referred to as a semiconductor device structure, that may be fabricated, at least in part, in accordance with the process of the present invention. Multi-layer structure 10 includes a semiconductor substrate 12 (e.g., a silicon wafer, ~~silicon-on-insulator~~ silicon-on-insulator (SOI), silicon-on-sapphire (SOS), silicon-on-glass (SOG), etc.), a field oxide layer 14 disposed on an active surface 13 ~~of the~~ of semiconductor substrate 12 and an active device region 16, polysilicon lines 18 disposed ~~on the~~ on active device region 16, ~~side wall~~ sidewall spacers 20 positioned on each side of the polysilicon lines 18, an intermediate structural layer 22 disposed over each of the foregoing elements, and a passivation layer 24 disposed over the intermediate structural layer 22. Passivation layer 24 is fabricated from doped silicon dioxide, such as BPSG, PSG or BSG. Intermediate structural layer 22 may be fabricated from either silicon nitride or undoped silicon dioxide.

Please amend the paragraph bridging pages 11 and 12 as follows:

FIG. 2 depicts masking of multi-layer structure 10 prior to defining a structure through passivation layer 24. A mask 26, which is also referred to as a protective layer, is layered and patterned over passivation layer 24. Mask 26 may be formed from a material such as a photoresist or other photoimageable material. Exemplary positive photoresists that are useful as mask 26 may include a novolac resin, a diazonaphthaquinone, and a solvent, such as n-butyl acetate or xylene. Exemplary negative photoresists that are useful as mask 26 may include a cyclized synthetic rubber resin, bis-arylazide, and an aromatic solvent. Such a mask 26 may be applied to, or coated onto, multi-layer structure 10 and

patterned by techniques that are known to those in the art, such as spin coating and photomask processing and patterning techniques. Alternatively, mask 26 may comprise an aerosol spray pattern of electrostatically chargeable hardenable liquid material, such as a polymer, which is not etched or is etched at a much slower rate than the underlying passivation layer 24. An exemplary method for spray-patterning such electrostatically chargeable hardenable liquid materials is described in United States Patent 5,695,658~~(the "'658~~ ("the '658 patent"), which issued to James J. Alwan on December 9, 1997, the disclosure of which is hereby incorporated by reference. Both photoresist materials (positive and negative) and non-photoimageable materials may be employed as mask 26 in accordance with the '658 patent. The utilization of masks 26 which comprise other~~non-photoimageable~~ non-photoimageable materials and the processes for applying and patterning them are also within the scope of the method of the present invention. The patterning of mask 26 defines openings 28, which are also referred to as apertures or contact apertures, therethrough, through which predetermined structures will be defined in the underlying passivation layer 24 during a subsequent etch step. Mask 26 comprises a material that is resistant to the etchant of the present invention (i.e., the etchant does not etch mask 26 or etches~~the mask~~ mask 26 at a relatively slow rate compared to the rate at which the etch substrate is etched). Thus, the areas of passivation layer 24 which underlie mask 26 are protected from the etchant during the subsequent etch step.

Please amend the first full paragraph appearing on page 12 as follows:

Turning now to FIG. 3, an etch is depicted, wherein an etchant 30, which is introduced into an etch chamber (not shown) either with or without a carrier gas, attacks the areas of passivation layer 24 that are exposed through openings 28 of mask 26. Dry etch processes that are known to those of skill in the art,~~including~~ including, without~~limitation~~ limitation, high density plasma etching, reactive ion etching (RIE), magnetic ion etching (MIE), magnetically enhanced reactive ion etching (MERIE), plasma etching (PE), point plasma etching, plasma enhanced reactive ion etching (PERIE), and electron cyclotron resonance (ECR), may be

employed with ~~the etchant of the present invention~~ etchant 30 and are within the scope of the process of the present invention. Etchant 30, which comprises a $C_2H_xF_y$-containing etchant of the present invention, etches an aperture through passivation layer 24 in a substantially vertical fashion until intermediate structural layer 22 is exposed. Intermediate structural layer 22, which is fabricated from either undoped silicon dioxide or silicon nitride, acts as an etch stop layer. Thus, etchant 30 etches intermediate structural layer 22 at a slower rate than the rate at which passivation layer 24 is etched. After the exposed areas of passivation layer 24 have been etched, mask 26 may be removed by processes that are known in the art, such as washing or etching techniques.

Please amend the paragraph bridging pages 12 and 13 as follows:

FIG. 4 illustrates a contact opening 32 or aperture, which is also referred to as a contact, that has been formed through passivation layer 24 by the etch process of the present invention. Contact opening 32 includes ~~side walls~~ sidewalls 34 that are substantially vertical relative to active surface 13 of semiconductor substrate 12. Contact openings 32 of the multi-layer structure 10 expose at least a portion of the intermediate structural layer 22 that lies above each of polysilicon lines 18, which may be logic circuits, such as word lines. Intermediate structural layer 22 defines a cap 36 over each polysilicon line 18. Thus, cap 36 may be fabricated from either undoped silicon dioxide or silicon nitride.